ARMY RESEARCH LABORATORY

GaN High Power Electronics

by Kenneth A. Jones, Timothy A. Walsh, Randy P. Tompkins, Iskander G. Batyrev, Michael A. Derenge, Kevin W. Kirchner, and Cuong B. Nguyen

ARL-TR-5455 **February 2011**

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14. ABSTRACT

This report details work from the Director's Strategic Initiative (DSI) on Gallium Nitride (GaN) High Power Electronics in which GaN devices are assessed compared to those fabricated from silicon carbide (SiC). For low power applications (<1500 V), GaN diodes have a lower on-resistance and less loss than their SiC counterparts because the critical breakdown field and electron mobility are larger. We expect this will also be true for high power electronic (HPE) GaN high electron mobility transistors (HEMTs) compared to SiC metal-oxide semiconductor field-effect transistors (MOSFETs). However, GaN devices are not yet manufacturable because the uniformity of the material across the wafer, and therefore the device properties, vary greatly. While the work at the U.S. Army Research Laboratory (ARL) does not yet match the best work being done in Japan, the reasons for this have been identified as the relatively large carbon background impurity concentration in traditionally grown metal-organic chemical vapor deposition (MOCVD) GaN films and the relatively large resistance of hydride vapor phase epitaxy (HVPE) GaN substrates. Using nontraditional MOCVD growth methods, more heavily doped HVPE GaN substrates, and GaN single crystals that have very recently become available, we expect be able to determine if a process can be developed to manufacture GaN devices that have superior properties to those made from SiC for some important Army applications.

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Gallium nitride, power electronics, diodes, transistors

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Contents

List of Figures

List of Tables

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1. Introduction

1.1 Rationale

Gallium nitride (GaN) high power electronic (HPE) devices have the potential to outperform those made from 4H-silicon carbide (SiC), the polytype used for HPE devices, because it has a larger critical electric field, ξ_C, the field at which the device breaks down –3.5 versus 2.5 MV/cm. This is due primarily to GaN's larger energy gap, E_G – 3.39 eV versus 3.25 eV. GaN also has a slightly larger electron mobility, μ – 930 versus 900 $cm^2/V{\cdot}s$.

These qualities enable GaN to theoretically have better device properties. One of these properties is the minimum thickness for the device, which is the width of the depletion layer when the device breaks down, W_B, so that the depletion layer will not 'punch through' the device before it breaks down. It can be expressed,

$$W_B = 2V_B/\xi_{C,} \tag{1}$$

where V_B is the breakdown voltage. The maximum doping level in the drift region, $n_{dmx} \alpha W_B^2$ so,

$$n_{dmx} = (\varepsilon\xi_C^2)/(2qV_B), \tag{2}$$

where ε is the electric permittivity. Thus, GaN can be more heavily doped. Combined with the higher mobility, this enables GaN to have a smaller specific on-resistance, $R_{ON{\cdot}sp}$, for a given V_B, where

$$R_{ON{\cdot}sp} = 4V_B^2/\mu\varepsilon\xi_C^3. \tag{3}$$

This is one of the most important parameters because it determines the loss when the device is turned on. As a result, the figure of merit (FOM) is defined as

$$FOM = V_B^2/ R_{ON{\cdot}sp}, \tag{4}$$

and it is illustrated in the theoretical plot of $R_{ON{\cdot}sp}$ versus V_B in figure 1, along with some of the better experimental values. Note that the experimental value recently achieved by the Japanese (*1*) exceeds the theoretical value for 4H-SiC, even though it was achieved using a relatively poor GaN substrate containing $>10^6$ dislocations/cm^2. The relative FOM (RFOM) is the ratio of the FOMs for a given material, and the value for GaN shown in table 1 is 2.75 times larger than it is for 4H-SiC even though the ratio of the critical fields is only 1.4 because $R_{ON{\cdot}sp} \alpha \xi_C^{-3}$.

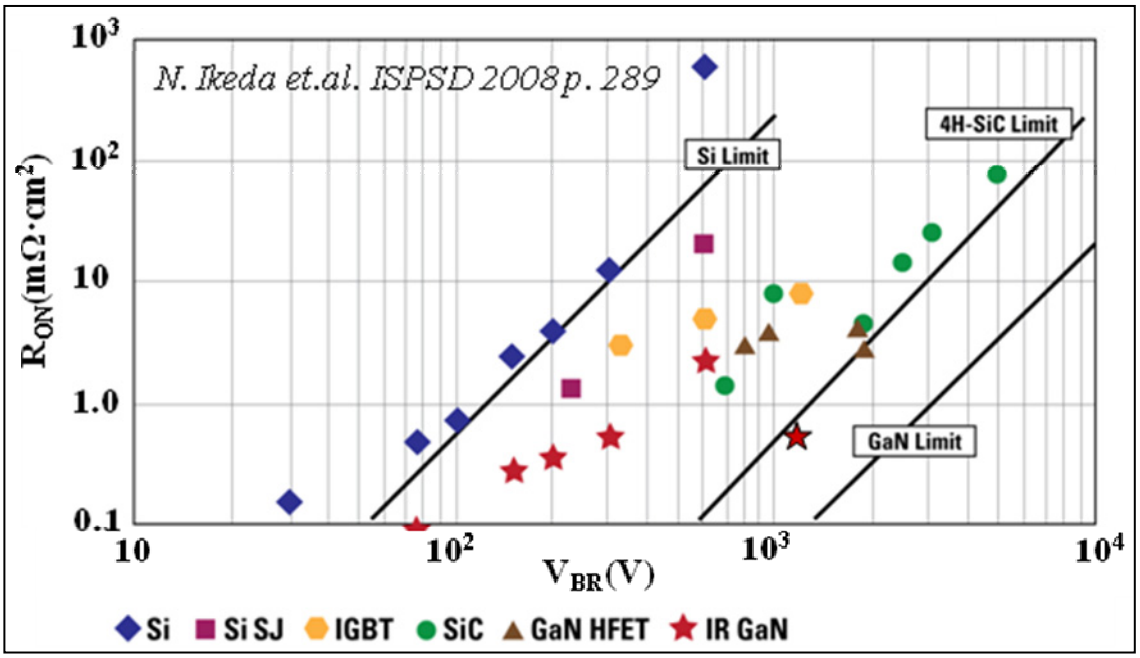


Figure 1. Plot of the theoretical specific on-resistance as a function of the breakdown voltage for silicon (Si), SiC, and GaN along with experimental values that have been obtained by a number of researchers.

Table 1. Values for some physical parameters for Si, 4H-SiC, and GaN.

	Si	SiC	GaN
$\varepsilon/\varepsilon_o$	11.8	9.7	9.5
$\mu_n(cm^2/V \cdot s)$	1100	900	930
ξ_C (V/cm)	.25 x 10^6	2.5 x 10^6	3.5 x 10^6
W_B (μm)	80	8.0	5.7
n_d (cm^{-3})	2.0 x 10^{14}	1.9 x 10^{16}	3.2 x 10^{16}
$R_{on \cdot sp}(m\Omega/cm^2)$	220	0.33	0.12
RFOM		667	1830

Another advantage GaN has is that it can form solid solutions with other group III elements, such as aluminum (Al), to form aluminum gallium nitride (AlGaN). The energy gap increases with the Al concentration, as does ξ_C, suggesting that AlGaN might be the HPE semiconductor material of the future following SiC/GaN. The ability to form a solid solution also increases the diversity of the devices one can fabricate. An important type of device is the high electron mobility transistor (HEMT), in which a two-dimensional electron gas (2DEG) with a larger electron mobility than is found in the bulk is created at the AlGaN/GaN interface. The mobility

is larger because the electrons are supplied by donors in the AlGaN, which are separated from the 2DEG so that they do not scatter the electrons as effectively. Also, the AlGaN/GaN interface can be very smooth, because the AlGaN grows epitaxially on the GaN and does not contain mismatch dislocations when its thickness is less than its critical thickness. This high mobility, which can be as large as 2500 $cm^2/V \cdot s$, can lead to a small channel resistance, a resistance that can dominate $R_{ON \cdot sp}$ for $V_B < 3000$ V.

On the other hand, SiC is a compound with a fixed composition. Second phases are formed, as opposed to solid solutions, when the group IV elements, carbon (C), Si, or germanium (Ge), are added to it. In order to form a 2DEG, a dielectric, usually silicon dioxide (SiO_2), has to be grown or deposited on the SiC. This complex interface contains many defects and can be rough, especially if the oxide is grown as it usually is, and they have so far limited the channel mobility to ~25 $cm^2/V \cdot s$. This limitation has caused the channel resistance to be the dominate resistance for $R_{ON \cdot sp}$ in the SiC metal-oxide-semiconductor field effect transistors (MOSFETs) that are currently being used.

Another advantage of GaN is that its dominant crystal structure is the hexagonal 2H structure. While the cubic 3C structure has been seen in stacking faults near the hetero-interface caused by the mismatch between the GaN film and the substrate, this phase is not nearly as stable as the 2H phase. Also, there is no evidence that applying a large current will alter the 2H phase. On the other hand, SiC has ~250 phases—sometimes called polytypes—of which the most common are the 3C, 4H, and 6H polytypes. These structures differ only in how their close packed planes are stacked on top of each other. 3C is said to have an AαBβCγAα…, 4H an AαBβAαCγAα… and 6H an AαBβCγAαCγBβAα… structure, where the Latin letter represents the Si atoms and the Greek letters represent the C atoms. The 4H structure is the desired structure for HPE electronics, and it has been shown that when large electrical currents are passed through it, the 4H structure is converted into 3C in some regions, and the associated stacking faults cause the on-resistance to increase with time (*2*). This problem can be minimized by greatly reducing the concentration of basal plane dislocations that catalyze the transformation from 4H → 3C, but this process is expensive.

The final advantage is that more money is being invested in GaN than any other semiconductor except Si because of the great interest in blue/ultraviolet (UV) emitters and detectors, and higher power radio frequency (RF) HEMTs. These considerable investments can be leveraged for GaN HPE.

1.2 Challenges

GaN device structures contain a large number of crystalline defects, most of which are dislocations created by the mismatch between the GaN film and the substrate on which it is grown. The structure is a heterostructure—that is, the film and substrate are different materials—and the difference in their lattice parameters is accommodated by the formation of misfit dislocations. Foreign substrates are required because, until very recently, large good

quality GaN crystals have not been grown. They cannot be grown in the traditional manner because GaN sublimates at normal pressures, and the nitrogen (N_2) partial pressure in equilibrium with the GaN is extraordinarily high at reasonable growth pressures (*3*). As a result, the GaN films are grown primarily on (0001) oriented sapphire (Al_2O_3), which has a 13% mismatch, or (0001) SiC, which has a 3.5% mismatch. Even though the dislocation concentration is larger at the film/substrate interface, a large number of dislocations, called threading dislocations, propagate through the film. Typically, there are ~10^9 threading dislocations/cm^2 in the GaN films grown by metal-organic chemical vapor deposition (MOCVD) and ~10^{10} in films grown by molecular beam epitaxy (MBE), when they are deposited on either substrate.

The challenges are to determine which types of dislocations are the most detrimental and reduce their concentration near the top surface of the GaN, where the devices are fabricated or the largest electrical stress is applied to them.

2. Approach

Our approach is to fabricate devices using the newly developed GaN substrates and compare them with devices made using GaN films grown on sapphire or SiC substrates. The devices being fabricated are Schottky diodes (SDs) and HEMTs, with the initial primary emphasis being on the SDs. The new substrates that are being investigated are ones being grown by hydride vapor phase epitaxy (HVPE) (*4*) and ammonothermal growth (*5*).

In HVPE growth thick GaN films are usually grown on sapphire substrates, and then the substrate is removed by rapidly heating the GaN film that absorbs light from a laser with a wavelength that is transparent to sapphire. The rapid thermal expansion of the GaN causes it to "pop off." This thick film is then used as a substrate for growing homoepitaxial GaN films that are >1 mm thick from which wafers can be cut. The process is illustrated in figure 2. The reason that the HVPE technique is used is because the growth rate is much faster than other growth methods. Typical HVPE growth rates range from 10–50 μm/h, which is high compared to an MOCVD growth rate of 12 μm/h and an MBE growth rate of 0.20.4 μm/h. The advantage of using these wafers is that they contain only ~10^6 dislocations/cm^2, as the threading dislocations tend to grow out of the films as they become thicker. However, in addition to containing a relatively large dislocation concentration, they also contain domains separated from each other by low angle grain boundaries (LAGBs), which can be formed by the bunching of some dislocations.

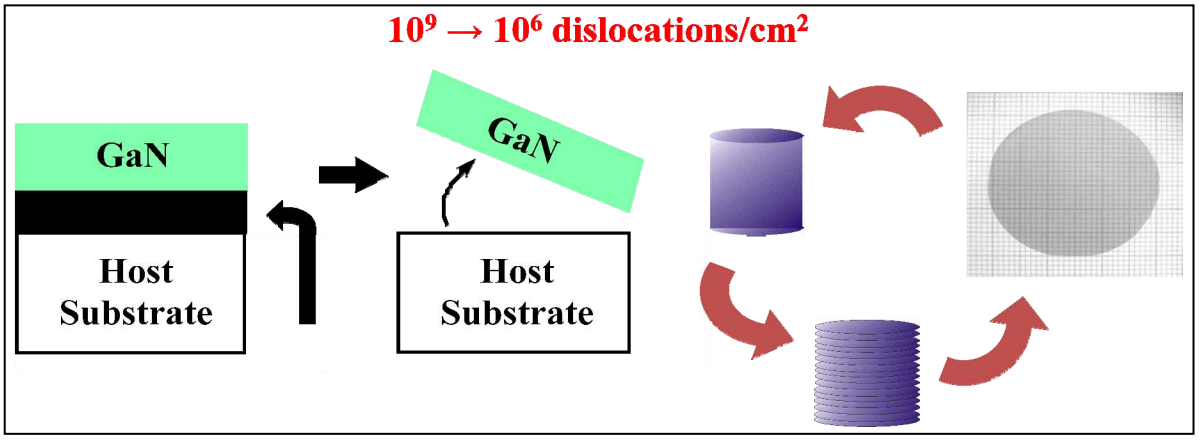


Figure 2. The process for creating wafers grown by HVPE.

The ammonothermal crystals are grown in an autoclave containing supercritical ammonia (NH_3), NH_3 at pressures where the vapor cannot be distinguished from the liquid, and GaN feedstock at pressures of 0.1–0.3 GPa and relatively low temperatures, 400–600 °C. The crystals that are grown can be as large as 2 inches in diameter, and they have very good crystal quality. They contain only ~10^3 dislocations/cm^2 and their x-ray rocking curve peak width can be as low as 16 in, compared to ~75 in for the best HVPE substrates and ~200 in for the best MOCVD films. In addition, they can be doped >10^{18} cm^{-3} and have a resistivity of 10^{-2} to 10^{-3} Ω·cm, which translates into a specific resistance of 0.35–0.035 mΩ· cm^2 for 350 µm thick wafers.

In the long term we would like to be able to grow AlGaN on high quality aluminum nitride (AlN) substrates in such a way that the dislocations are confined to the region of the interface, and only a few propagate up to the AlGaN surface where the devices are fabricated and/or the high electrical stress points occur. This would enable us to grow AlGaN of any composition with low concentrations of dislocations for any Al content. This has already been achieved in silicon-germanium (SiGe) film growth on Si substrates by grading the SiGe layer or growing superlattice steps with an increasing Ge concentration (*6*). This work is being pursued under a Director's Research Initiative (DRI) with the possibility that it will be transferred to the multi-scale modeling program. This work would couple nicely with this DSI.

3. Results

3.1 Schottky Diodes

Schottky diodes were fabricated on unintentionally doped (UID) GaN films grown on a sapphire or HVPE GaN substrate to a thickness of ~6 µm, and the results are compared. UID films were used because the literature shows that typically such films are doped n-type with Si and/or oxygen (O) to ~10^{16} cm^{-3}. This value is ~10^2 larger than it is for gallium arsenide (GaAs)

because the growth temperature for GaN is substantially higher, ~1050 °C, compared to ~600 °C for GaAs. Higher temperatures are required because the hydrogen (H) is more strongly bonded to the N in NH_3 than it is bonded to the arsenic (As) in arsine (AsH_3). In addition, NH_3 is not generally as pure as AsH_3, because purity in GaN is not yet as important an issue as it is for GaAs.

The comparisons must take into account that the diodes are fabricated differently because, being an insulator, current cannot be passed through the Al_2O_3. As a result contacts have to be made to a heavily doped (~10^{19} cm^{-3}) GaN film by etching down to it, as illustrated in figure 3a. On the other hand, no etching is required to fabricate the SD on the GaN film grown on the GaN substrate because it has a backside contact, as shown in figure 3b. The good news for the SD on the sapphire substrate is that there is no substrate resistance. The bad news is that it takes a considerable amount of time to etch down 6 µm, the exposed sidewalls can contain defects that cause premature breakdown, and the etch can damage the surface of the n^+ film making it more difficult to contact. In addition the geometry of the SD on sapphire causes current crowding making it difficult for it to carry large amounts of current. The good news for the SD on a GaN substrate is that no etching is required and the current carrying capacity is not limited by geometry. The bad news is that the substrate adds a series resistance to the device, thereby increasing $R_{ON \cdot sp}$.

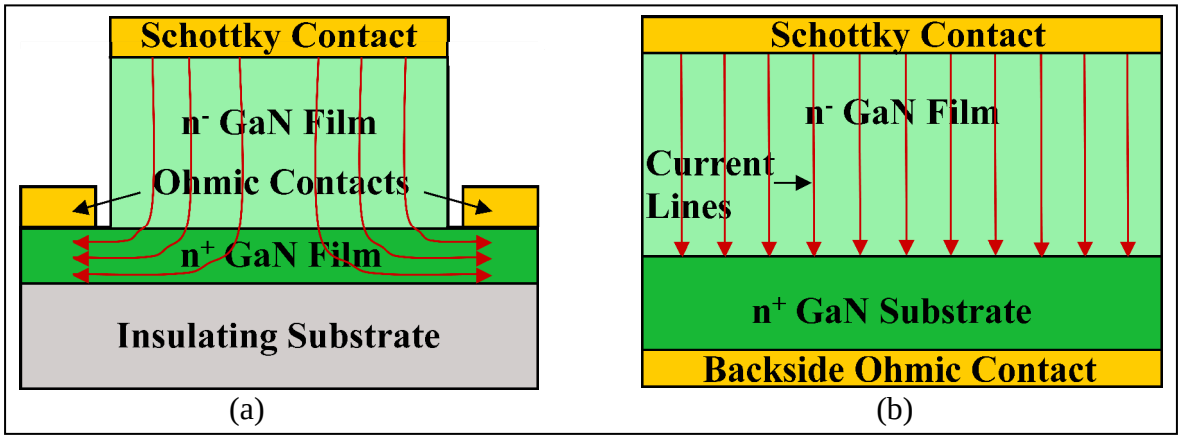


Figure 3. Schematic diagrams of SDs with (a) front side contacts and an insulating substrate, and (b) backside contacts and a conducting substrate.

As shown in figure 4, the initial results for the *i*-V and C-V (red 100 Torr line only) were discouraging. The diodes did not even turn on until V > 10 V and the *i*-V curves had large hysteresis no matter what temperature they were measured at. In addition, the reverse C-V characteristics showed that the capacitance did not vary with the voltage and it was small, which is indicative of the material being an insulator. It was also difficult to impossible to make ohmic contacts to the films again suggesting they were insulators. The results were not affected by which substrate was used, or who grew the film, as films grown at the U.S. Army Research

Laboratory (ARL), State University of New York (SUNY)-Albany, Sandia National Laboratories, and Penn State all showed the same results.

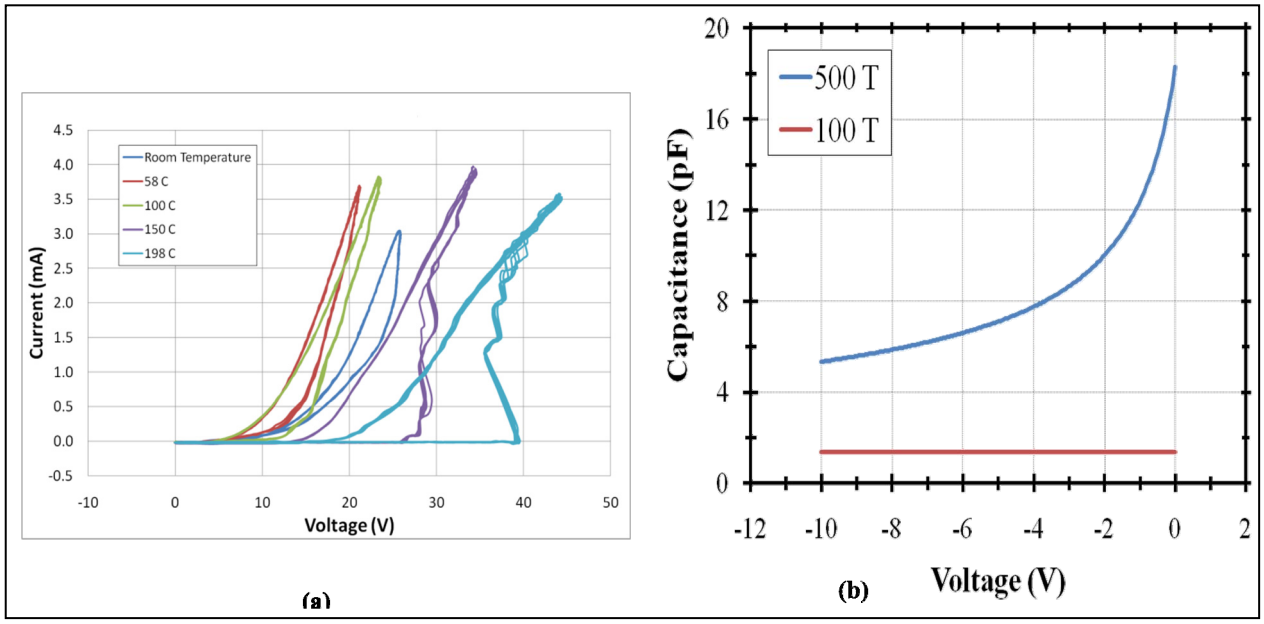


Figure 4. Example of the initial (a) *i*-V and (b) C-V curves for films grown on any substrate.

We were able to make our films conducting by doping them slightly with Si using silane (SiH_4) as the source in our MOCVD system. C-V measurements showed that the net n-type doping concentration was 5.2 x 10^{16} cm^{-3}, and, as shown in figure 5a and table 2a, the representative diode had adequate characteristics. The forward voltage, V_F, the voltage when the current density of the diode is 100 A/cm^2, was 2.92 V. Although reasonable it suggests the diode is more resistive than one would predict from the doping concentration. That is, in fact, the case, as $R_{ON\cdot sp}$ = 6.46 $m\Omega\cdot cm^2$, which is the result of a lower than expected carrier mobility. This results in a low FOM = 2.4 MW/cm^2 because the breakdown voltage, V_{BR} = 124 V, is low due, in part, to the relatively high doping.

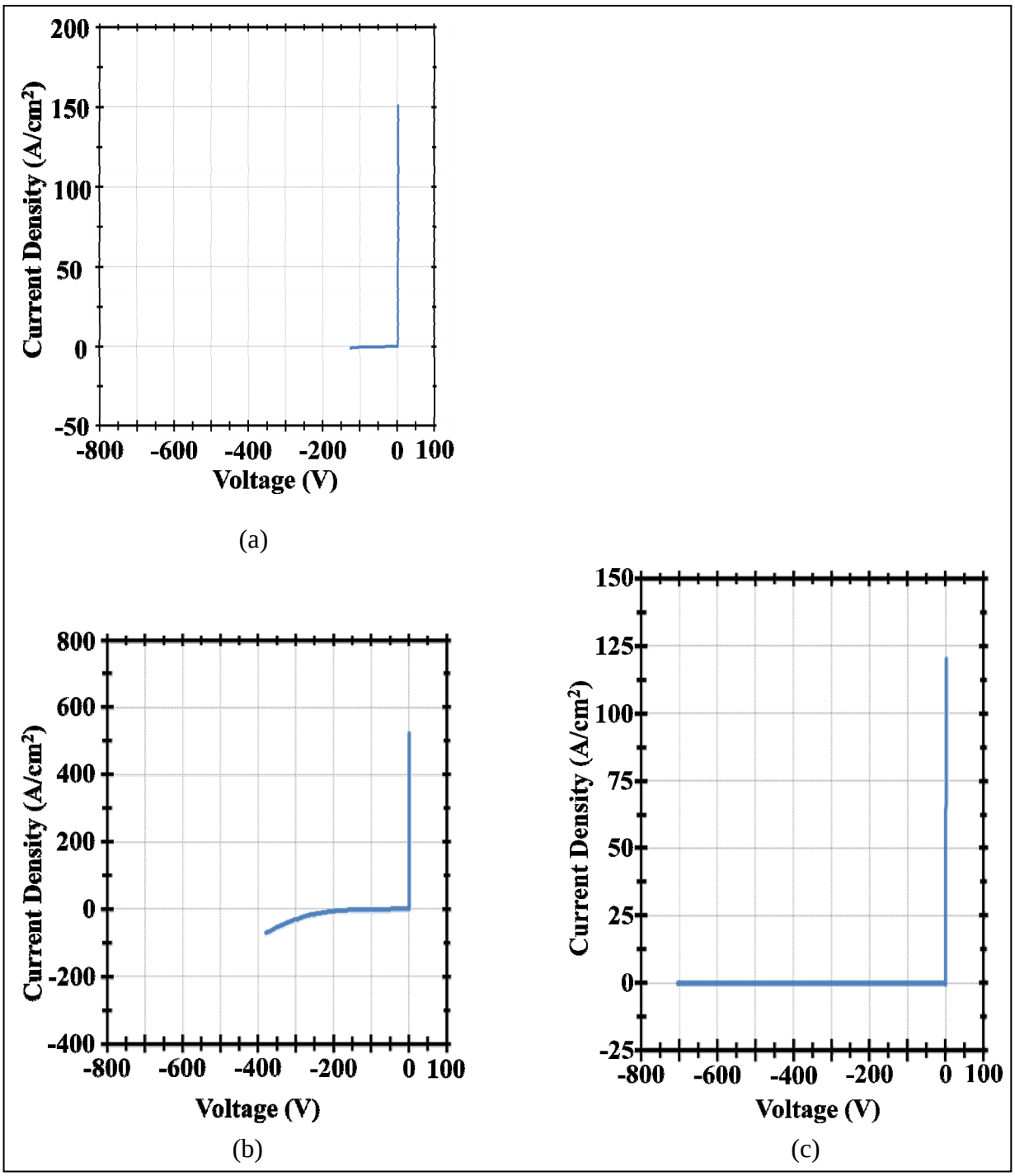


Figure 5. *i*-V curves for SDs fabricated from (a) MOCVD film Si-doped to 5.2 x 10^{16} cm^{-3}, (b) HVPE GaN substrate doped 1.6 x 10^{16} cm^{-3}, and (c) HVPE GaN substrate doped 3.9 x 10^{15} cm^{-3}.

Table 2. Electrical parameters for SDs fabricated from (a) MOCVD film Si-doped to 5.2 x 10^{16} cm^{-3}, (b) UID MOCVD film grown on sapphire at 500 Torr, (c) HVPE GaN substrate doped 1.6 x 10^{16} cm^{-3}, and (d) HVPE GaN substrate doped 3.9 x 10^{15} cm^{-3}.

V_f (100 A/cm^2)	2.92 V
Ideality factor	3.69
Barrier height	0.84 eV
On resistance	6.46 mΩ·cm^2
$J_{leakage}$ (100 V)	365 mA/cm^2
Max reverse voltage	124 V
Max reverse current	845 mA/cm^2
FOM V_B^2/R_{on}	2.4 MW/cm^2
n_d	5.2 x 10^{16} cm^{-3}

(a)

V_f (100 A/cm^2)	0.74 V
Ideality factor	1.02
Barrier height	0.94 eV
On resistance	0.29 mΩ·cm^2
$J_{leakage}$ (100 V)	0.26 mA/cm^2
Max reverse voltage	274 V
Max reverse	346 mA/cm^2
FOM V_B^2/R_{on}	261. MW/cm^2
n_d	1.2 x 10^{16} cm^{-3}

(b)

V_f (100 A/cm^2)	.78 V
Ideality factor	1.11
Barrier height	0.88 eV
On resistance	0.96 mΩ-cm^2
$J_{leakage}$ (100 V)	22.72 mA/cm^2
Max reverse voltage	380 V
Max reverse current	72 A/cm^2
FOM V_B^2/R_{on}	151. MW/cm^2
n_d	1.6 x 10^{16} cm^{-3}

(c)

V_f (100 A/cm^2)	1.72 V
Ideality factor	1.13
Barrier height	0.87 eV
On resistance	10.68 mΩ·cm^2
$J_{leakage}$ 100 V	0.01 mA/cm^2
Max reverse voltage	704 V
Max reverse current	1.10 mA/cm^2
FOM V_B^2/R_{on}	46.4 MW/cm^2
n_d	3.9 x 10^{15} cm^{-3}

(d)

The values of other parameters used to characterize SDs are consistent with the analysis that the material could be highly compensated, which would account for the low electron mobility. One of these values is the semiconductor ideality factor, *n*. It appears in the equation for the forward current in the diode,

$$i \approx I_o e^{-qV/nkT}, \quad (5)$$

where I_o is the ideal reverse saturation current, *q* is the charge on an electron, *k* is Boltzmann's constant, and T is the absolute temperature. *n* is used to account for imperfections in the conducting process such as generation-recombination centers in the depletion region. For the

ideal diode, $n = 1$, and diode quality is measured by how close the experimental value approaches it. The experimental value of 3.69 for this diode is very large, and it suggests that GaN contains a large number of detrimental electrically active point defects.

Another parameter used to assess the diode quality is the barrier height, $ø_b$. The ideal value is the difference between the Fermi energies of the metal and semiconductor, but defects, such as those that enable tunneling through the barrier created by the Fermi level difference, cause the experimental value to be smaller. The value for this diode is 0.84, which is adequate, but a little low. This supports the hypothesis that the material does contain a number of electrically active point defects.

A search of the literature suggested that C was the culprit, as a theoretical analysis showed it can act as a deep acceptor 0.90 eV above the valence band (*7*). It is difficult to tie this down because C is amphoteric in that it could substitute for an N atom and act as an acceptor or substitute for a Ga atom and act as a donor. Which site it is more likely to occupy depends on where E_F lies. When E_F is small, C is more likely to occupy a Ga site and act as a donor. On the other hand, when E_F is large, as it is in n-type material, C is more likely to occupy a N site and act as an acceptor, i.e., C tends to compensate the dopant whether it is a donor or an acceptor.

The likely source for the C is the organometallic, trimethyl gallium [$(CH_3)_3Ga$], which is the source for the Ga used to grow the films. It is more of a problem for GaN than for GaAs because, as noted earlier, GaN has to be grown at a higher temperature.

A search of the literature showed experimentally that C can become incorporated to concentrations $>10^{16}$ cm^{-3} for MOCVD films grown on sapphire (*8, 9*), as determined by secondary ion mass spectroscopy (SIMS). However, it can be reduced by growing the films at higher pressures. It was hypothesized that the lower C incorporation is due to the material being of better crystal quality when it is grown at the higher pressure, as the grain size is larger and the dislocation concentration is smaller (*8*). That the crystal quality plays a role in the incorporation of C is supported by the observations that 5×10^{16} cm^{-3} of C was incorporated into a film grown on sapphire, while under the same growth conditions the C concentration was at or below the concentration level (*1*) that can be detected by SIMS (*10*), which is 1 to 2×10^{16} cm^{-3} for films grown on HVPE GaN substrates that contain $\sim 10^3$ fewer dislocations.

This issue was not clarified earlier because device structures grown for blue/UV detectors and emitters or RF HEMTs are always doped at levels $>10^{17}$ cm^{-3}. This is somewhat like discovering there are small leaks in a system after one has fixed the larger ones! Also, most growers for these devices grow at the lower pressure of 100 Torr, because the growth rate is faster. This rate has been attributed to more pre-reactions is the gas phase before the nutrients reach the growth surface, since the number of molecular collisions is proportional to the pressure (*11*).

Further testing suggests that background C is indeed the problem, as the results for devices fabricated from films grown at 500 Torr listed in table 2b and the C-V curve (blue line) in figure 4b are consistent with our hypothesis. The C-V curve is typical for a semiconductor diode in that the capacitance decreases as the reverse bias increases. It was also used to determine the carrier concentration of 1.2×10^{16} cm^{-3}. $V_F = 0.74$ V suggests that the electron mobility is higher because there are fewer detrimental point defects. This is further confirmed by a low $R_{ON \cdot sp} = 0.29$ m$\Omega \cdot$cm^2, which along with a $V_{BR} = 274$ V yields an FOM = 261 MW/cm^2, which is more than 10^2 larger than it was for the intentionally Si-doped sample with a film grown at 100 Torr. V_{BR} is lower than expected, but that could be due to the fact that the device was a front-side diode that had to be etched. Also, with $n = 1.02$ and $\phi_b = 0.94$ eV, the diode almost has an ideal metal semiconductor interface.

Thinking there would be less C in the HVPE substrates because the Ga source does not contain C—the source is gallium chloride (GaCl)—we fabricated SDs directly on the substrates. The results shown in figure 5b and table 2c are very encouraging. The first substrate was found to have a doping concentration of 1.6×10^{16} cm^{-3} from C-V measurements, and $V_F = 0.78$ V. Though larger than the value found for the diode that was fabricated from the GaN film grown at 500 Torr, it is still considered to be a good value. The larger voltage is probably due to the series resistance of the substrate, and this is confirmed in the value of $R_{ON \cdot sp} = 0.96$ m$\Omega \cdot$cm^2. Even though $V_{BR} = 380$ V is larger than it was for the high pressure film growth, the FOM = 151 MW/cm^2 is smaller due to the larger $R_{ON \cdot sp}$. The ideality factor, $n = 1.11$, is a little larger and the barrier height, $\phi_b = 0.88$ eV, is a little smaller implying that the metal-semiconductor interface, while good, is not as good as it was for the high pressure growth diode. This is probably due to the fact that the semiconductor surface was a polished surface, as opposed to a virgin film surface, so it is likely the interface contained a few more defects.

To try to increase the breakdown voltage, we searched for a substrate with a lower doping level so the ξ-field in the depletion layer for a given voltage would be lower. We found one with a net carrier concentration of 3.9×10^{15} cm^{-3} using C-V measurements. We were able to achieve $V_{BR} = 704$ V, but that came at a cost of increased $R_{ON \cdot sp} = 10.68$ m$\Omega \cdot$cm^2 due to the larger series resistance of the lower doped substrate. The higher resistance is also reflected in the larger $V_F = 1.72$ V and the smaller FOM = 46.4 MW/cm^2. The values of $n = 1.13$ and $\phi_b = 0.87$ eV are virtually the same as they were for the higher doped sample, suggesting that the doping level is not a factor that affects them.

The values listed thus far have been for the better diodes; they are not necessarily representative, as there are large variations across the wafer. To illustrate this, we first turn to the layout of the diodes in a 2 × 2 mm cell shown in figure 6a. Each cell contains forty-two 30 µm, twenty 100 µm, twelve 200 µm, and ten 300 µm devices, and each 1 × 1 cm GaN wafer contains a 4 × 4 array of cells as shown in figure 6b. The crystals were also divided up into four areas, as shown in figure 6c, that were individually interrogated using x-ray rocking curve, scanning electron microscopy (SEM), and atomic force microscopy (AFM) analysis. The samples with GaN films

grown on sapphire wafers were quartered as shown in figure 6d, and the four regions in each quarter with equal areas except for Area I, which is larger, that were individually investigated using x-ray rocking curves, SEM, and AFM are also delineated.

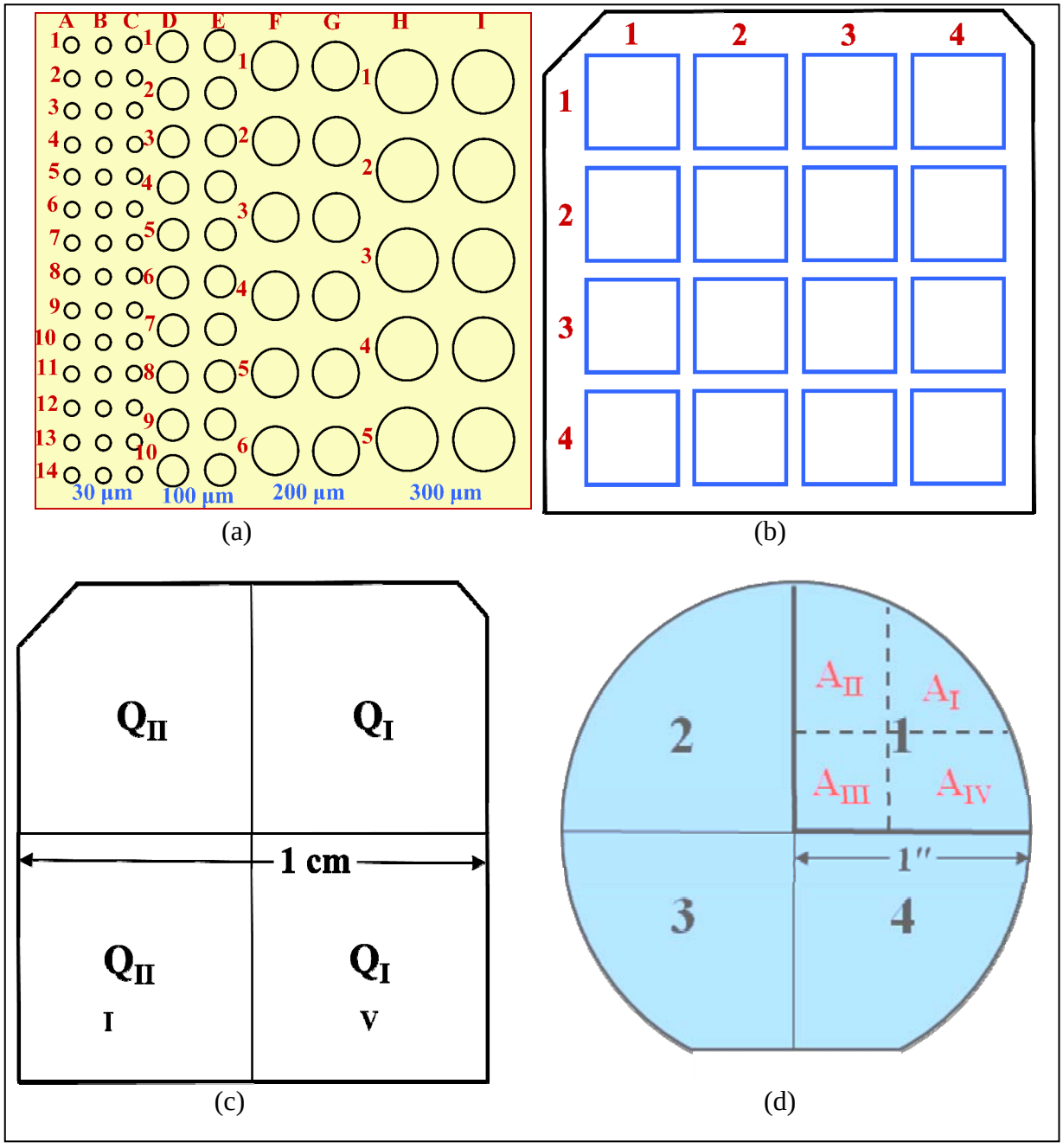
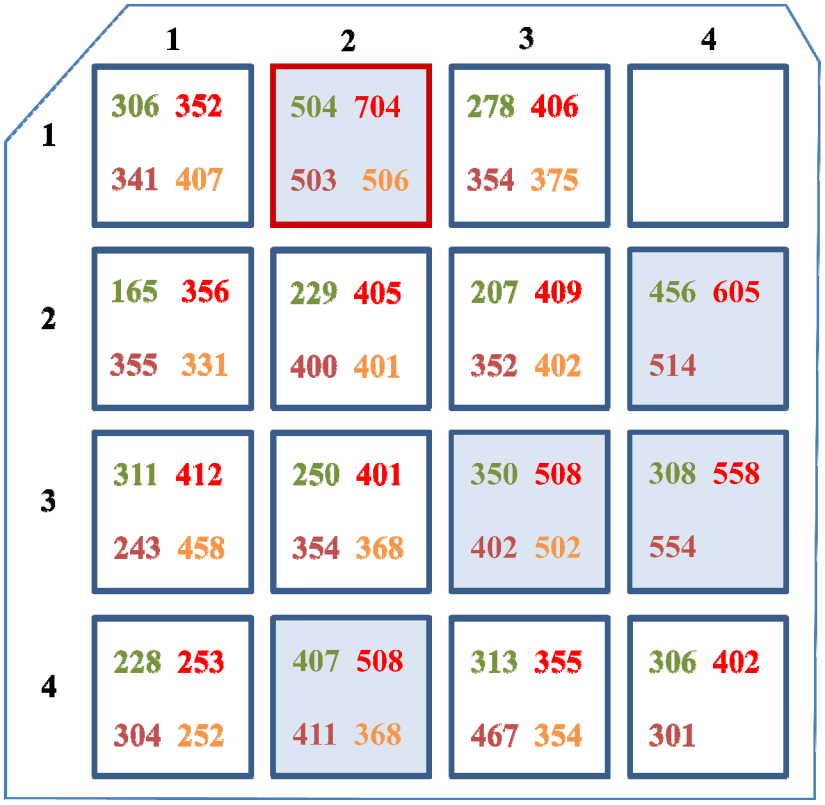


Figure 6. (a) Layout of the diodes in a unit cell. (b) Layout of the cells on ~1 × 1 cm wafer. (c) The four quarters of a 1 × 1 cm wafer. (d) The four quarters of a 2 in diameter wafer, and the four quarters within a quartered wafer.

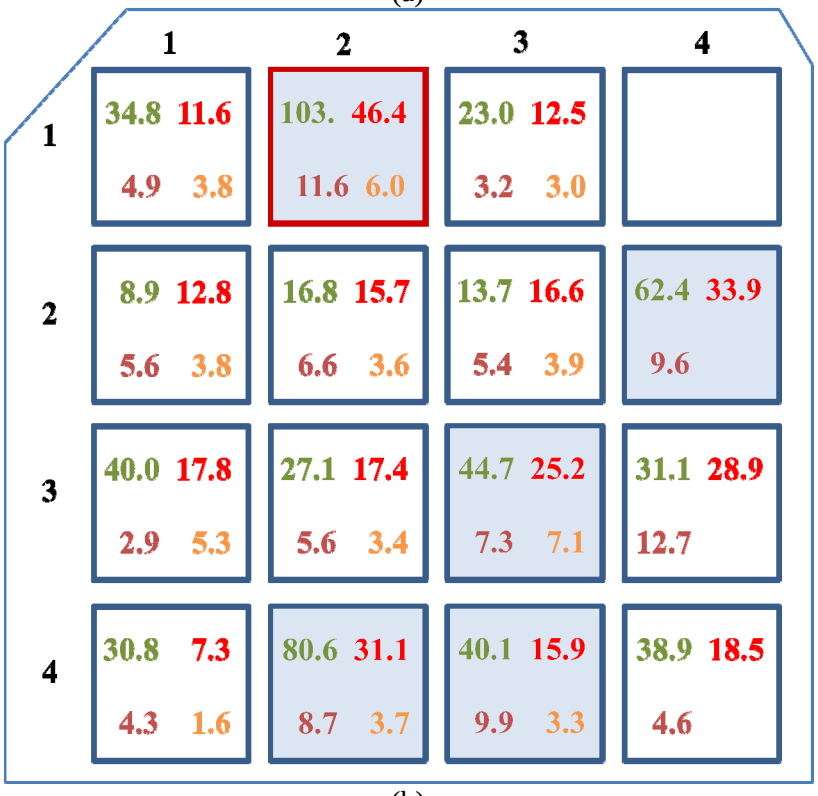
The values for the largest V_{BR} in each cell for each diode diameter of 30, 100, 200, or 300 µm are listed sequentially in table 3a, and the largest FOMs are listed in table 3b for the diodes fabricated on the more lightly doped HVPE GaN substrate. The diode with the largest V_{BR} = 704 V is the 100-µm diode in the upper left cell outlined in red. The maximum V_{BR} for the diodes with other diameters are 504 V (30 µm), 554 V (200 µm), and 506 V (300 µm). The 100-µm-diameter diode has the largest value, 11 out of 15 times. We hypothesize this is the case because the larger diodes are more likely to lie above a defect that can cause premature breakdown. This, in fact, was shown to be the case for SiC diodes being fabricated ~10 years ago. The smallest diode does not have the largest V_{BR} because it has the largest circumference to area ratio, and devices are more likely to break down at the edges. The maximum V_{BR} for the 100-µm diodes ranges from 704 to 165 V, and the average is 416 V. One cannot completely rule out process variations, but it is much more likely that these large variations are due to material variations across the wafer.

The diode with the maximum FOM is the 30-µm diode in the same cell, and its value is 103 MW/cm^2. This is a result of its $R_{ON\cdot sp}$ being smaller, which is somewhat deceptive because the calculations do not take into account the current spreading between the Schottky and backside contacts, and the spreading is the largest in the smallest diodes. This is probably why the 30-µm diode has the largest value, 13 out of 15 times. Again there is a large variation, as the lowest value is 8.9, and the average is 39.7 MW/cm^2. The maximum values for the other diodes are 46.4 (100 µm), 11.6 (200 µm), and 6.0 (300 µm).

Table 3. The maximum values for (a) V_{BR} and (b) FOM in each cell of each diode diameter of 30, 100, 200, or 300 μm.



(a)



(b)

The distribution of V_{BR} for the more heavily and more lightly doped GaN substrates are shown in figure 7. For the more heavily doped substrate, which has the smaller V_{BR}, the smallest diode has the largest values. For the more lightly doped sample the larger diodes have the larger V_{BR}, suggesting a larger circumference to area ratio has a more detrimental effect at higher V_{BR}.

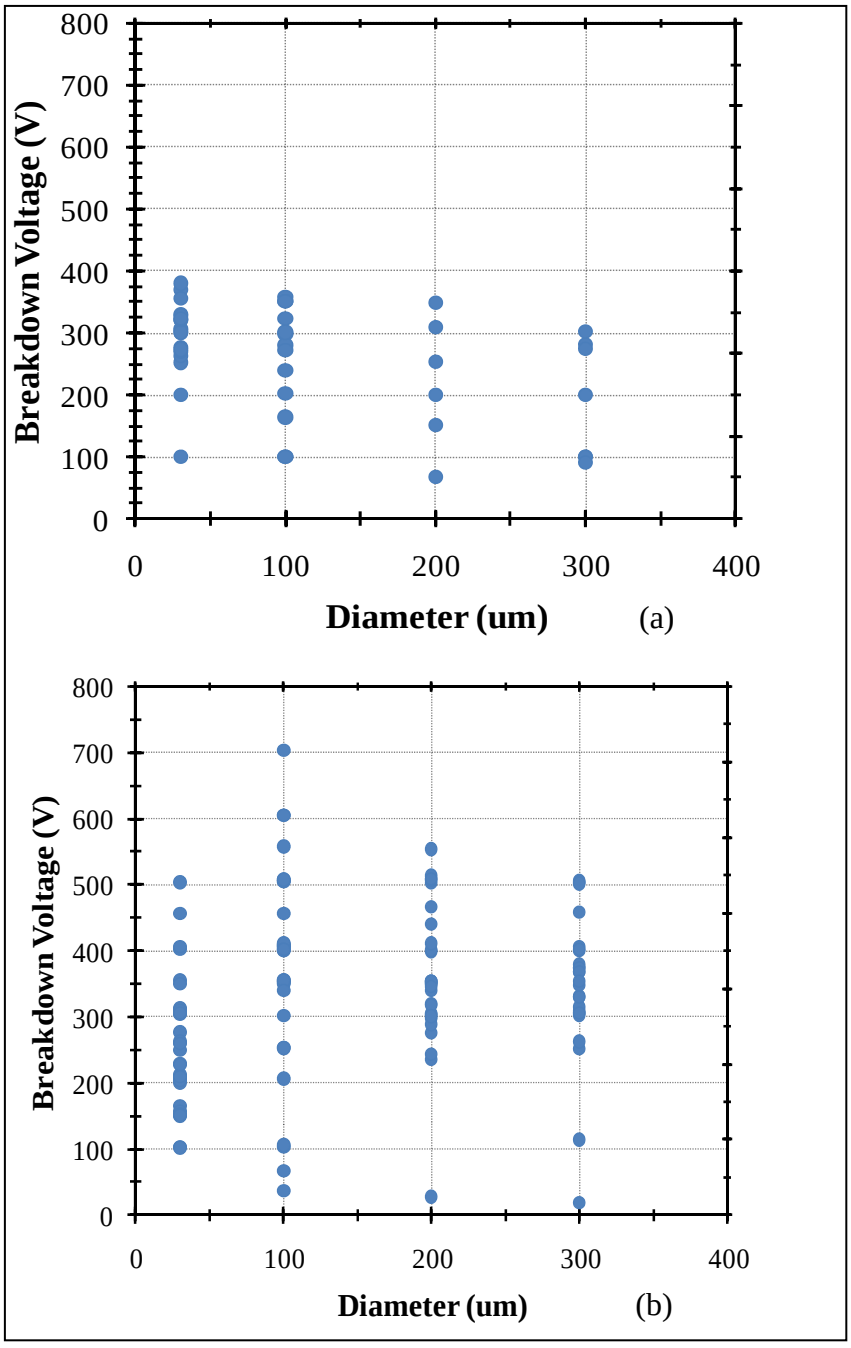


Figure 7. The distribution of V_{BR} for diodes with different diameters for the (a) more heavily, and (b) more lightly doped GaN substrate.

The plots of $ø_b$ versus *n* for the more heavily and more lightly doped GaN substrates are shown in figure 8. In general, the barrier heights and ideality factors correlate in that the diodes with the larger $ø_b$ have the smaller *n*. The more heavily doped substrate has more data points near the ideal values, indicating its crystal quality or preparation was better. Also, the parameters appear to be less diameter dependent suggesting the crystal has better quality.

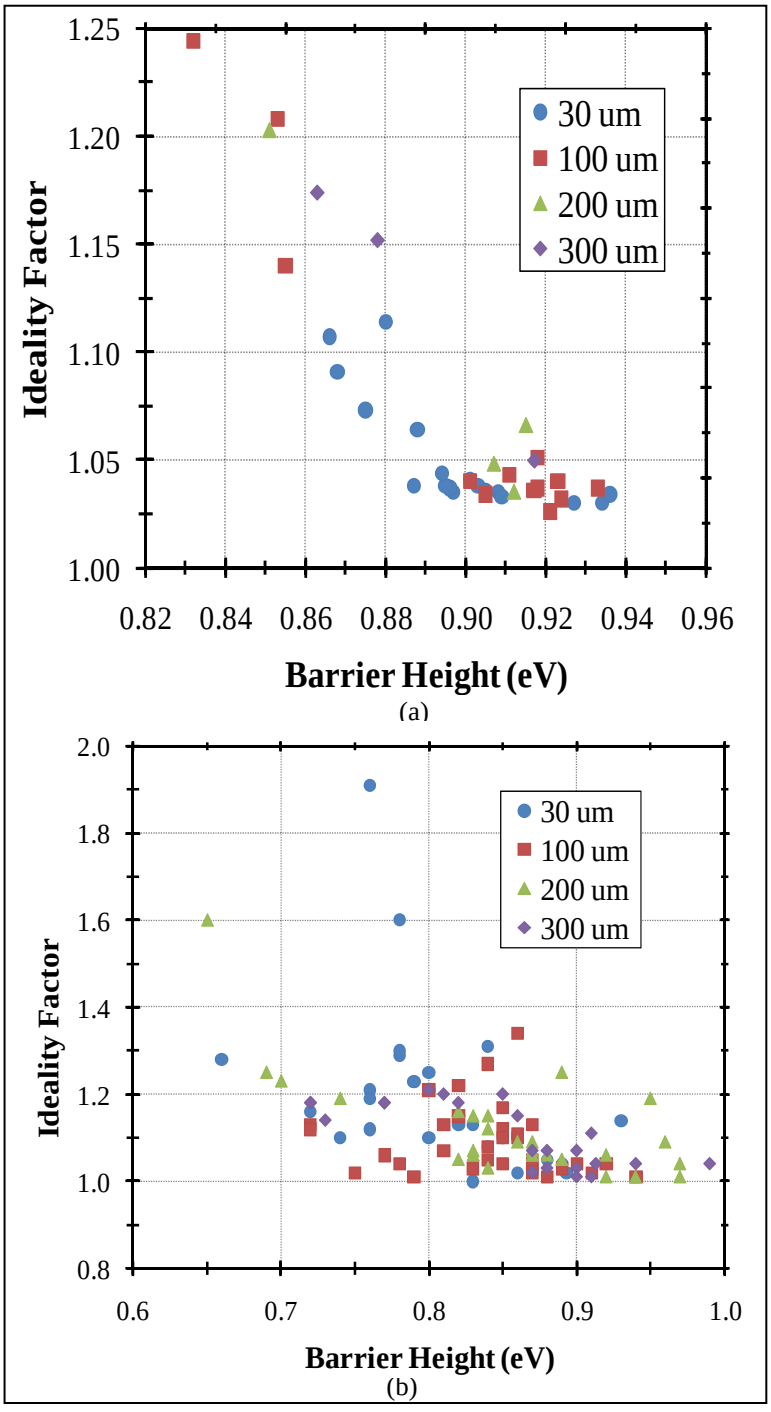


Figure 8. Plot of $ø_b$ vs. *n* for diodes with different diameters for the (a) more heavily and (b) more lightly doped GaN substrate.

The x-ray rocking curve analysis in figure 9 also shows that the more heavily doped GaN substrate has better crystal quality in that the rocking curve peak widths are thinner. The variation in the asymmetric peak widths also shows that the crystal quality is not uniform, and that the more heavily doped wafer appears to have the greatest variation. However, the apparent crystal quality does not correlate well with the regions where the largest breakdown voltages, as indicated by the shaded cells, occur. It is likely this is due to the fact that the x-ray line, whose dimensions are 3 × 0.35 mm, samples an area that is too large. We will continue to use x-ray rocking curves to monitor crystal quality, but we plan to try to correlate the device properties with the distribution of individual dislocations as determined by non-destructive electron channeling contrast imaging (ECCI), AFM, Kelvin probe, and cathodoluminescence (CL), and destructive etch pit analysis.

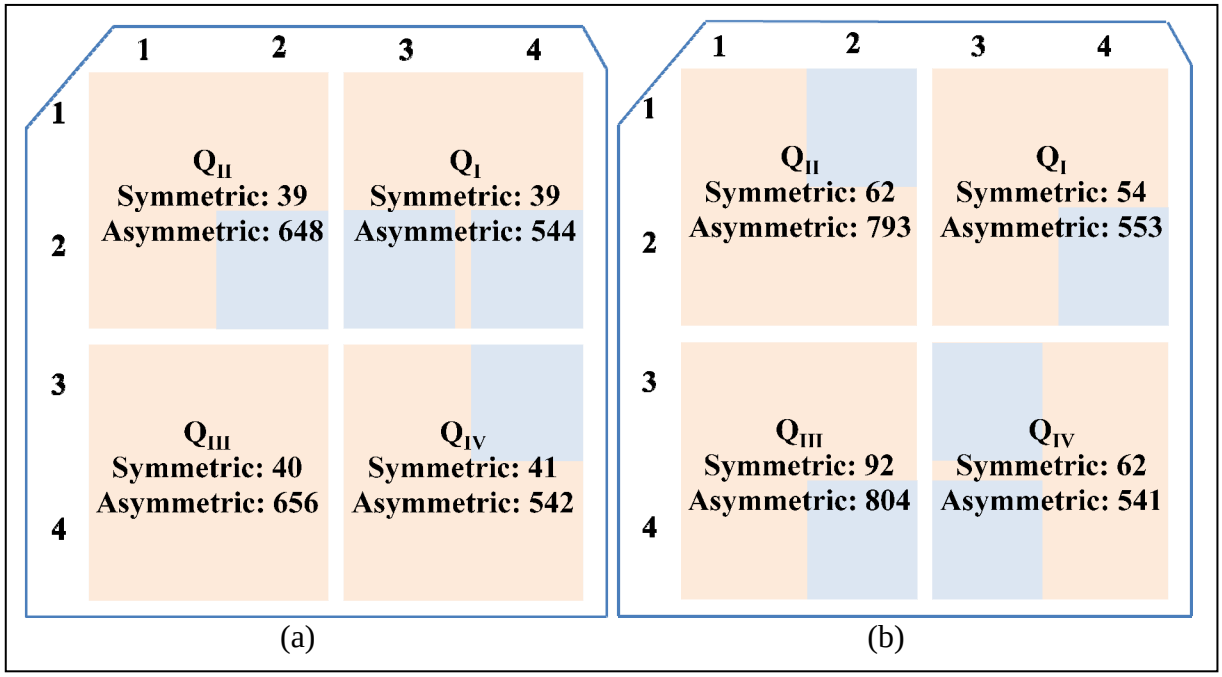


Figure 9. The x-ray rocking curve peak widths for the symmetric and asymmetric reflections in each of the four quarters of the wafer for the (a) more heavily and (b) more lightly doped GaN substrates.

3.2 Ion Implantation

Schottky diodes, especially at larger V_{BR}, have a tendency to have large leakage currents. This problem to some extent has been addressed for Si and SiC diodes by creating the junction barrier Schottky (JBS) diode in which the diode acts like a SD with a small V_F under forward bias and like a p-n diode with a low leakage current under reverse bias. They are made by ion implanting p-type channels into the n^- drift layer that are ~3 μm apart. The challenge is to be able to activate the implants and remove the implant damage. The process requires high annealing temperatures, T_A, and at these high temperatures N can preferentially evaporate and destroy the surface. We have developed an AlN annealing cap that to some extent avoids this and are in the

process of obtaining a patent for it. We obtained a good result for activating the n-type dopant Si with 70% activation at 1250 °C (*12*).

However, we were unable to replicate these good results for magnesium (Mg) p-type implantation. When we implanted the UID sample with Mg, we were unable to make it p-type by annealing it, and when we implanted a sample that was already doped with Mg *in situ*, the hole concentration dropped. Using transmission electron microscopy (TEM), we discovered that stacking faults (figure 10a) were formed by the implant/anneal process, and that they could not be annealed out. This suggests that the Mg implant stabilizes the stacking fault. We performed density functional theory (DFT) calculations on the electronic effects of the stacking faults and found that they created deep donor states 0.7–0.8 eV above the valence band, as illustrated in figure 10b. They can act as acceptor traps, which can account for the decrease in the hole concentration in the implanted samples. This work has been submitted for publication (*13*).

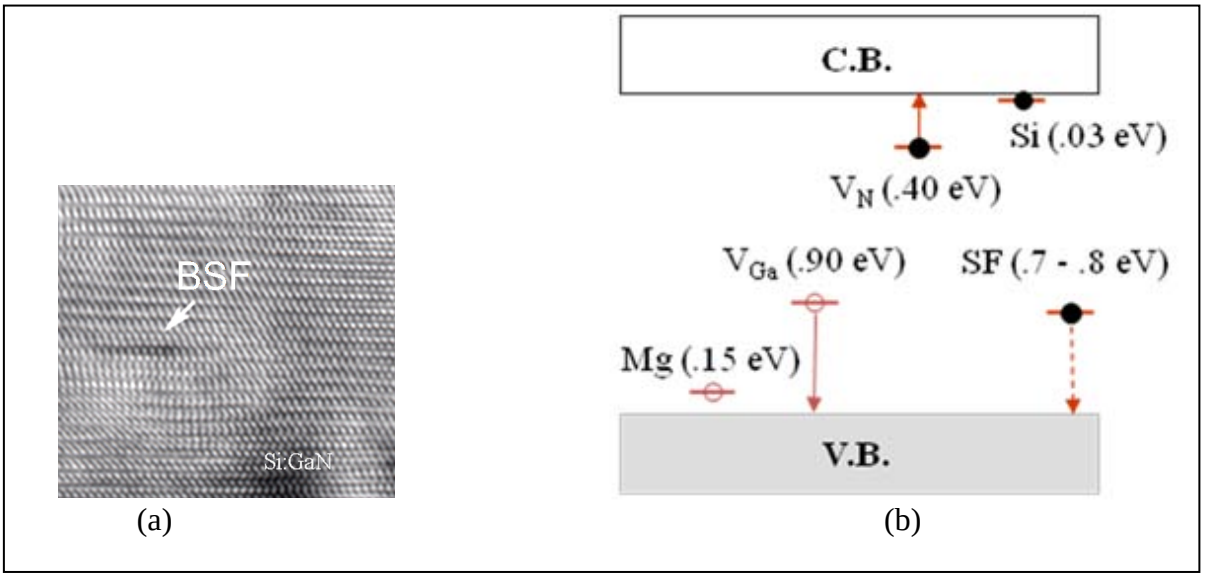


Figure 10. (a) TEM of a stacking fault produced by ion implantation and (b) the deep donor state associated with them as predicted by our DFT modeling.

We were successful in using our implant process for n-type implants to lower the specific contact resistance, ρ_c, to n-type samples (*14*). This will not have implications for SD technology because the regions that are contacted are heavily doped, but for HPE HEMT technology it could be a great benefit because contacts are made to a low doped region. The regions where the contacts are made could be locally doped using ion implantation, which enables the contact to have a lower resistance. In one set of samples we made shallow Si implants beneath the regions where the contact pads were to be evaporated into two wafers; one was *in situ* doped to 3.56×10^{17} cm^{-3}, and the other was doped to 6.67×10^{16} cm^{-3}. The other set of samples was not implanted. Both sets of samples were capped and annealed at T_A from 1100–1250 °C for 2, 5, or 10 min, and then the cap was selectively removed in warm potassium hydroxide (KOH). Titanium (Ti)/Al contact metals were evaporated, and then they were annealed for 5 min at

730 °C to form the contact. In the results shown in figure 11, the implanted samples had a smaller ρ_c in those that were annealed at T_A > 1100 °C, and the best results were obtained for the samples annealed at 1200 °C for 10 min. We achieved the lowest contact resistance on record with a value of 2.2 x $10^{-8}\Omega \cdot cm^2$ for the sample doped to 3.56 x 10^{17}. Mr. Cuong Nguyen reported on this work at the International Semiconductor Device Research Symposium, where he won the best student poster award.

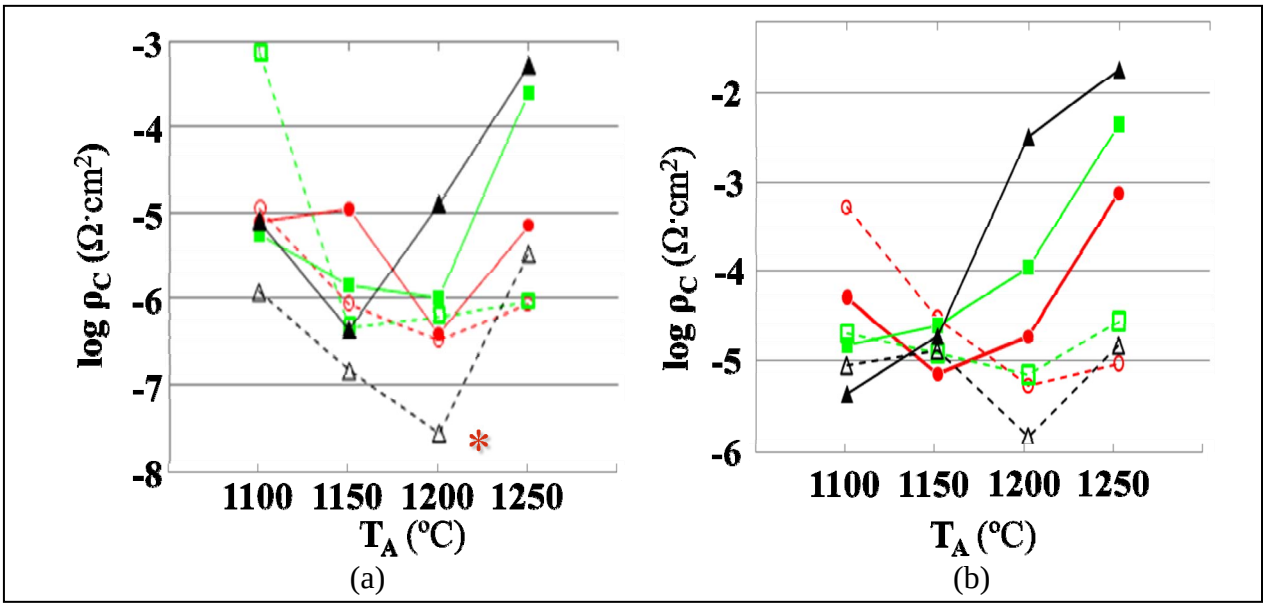


Figure 11. Contact resistance plotted as a function of the annealing temperature for a sample doped to (a) 3.56 x 10^{17} or (b) 6.67 x 10^{16} cm^{-3}. Broken lines (– – – –) represent implanted samples; solid lines (————) represent samples that were not implanted. Circles (○●) represent samples annealed for 2 min, squares (□■) for 5 min, and triangles (△▲) for 10 min.

3.3 HPE HEMTs

As mentioned in section 1, the attraction of HPE HEMTs like the one displayed in figure 11 is that they should have a smaller $R_{ON \cdot sp}$ due in part to the high electron mobility in the 2DEG. Recently, researchers at Panasonic have achieved $R_{ON \cdot sp}$ = 2.6 $m\Omega \cdot cm^2$ with a HEMT that had a V_{BR} = 800 V, and researchers at IMEC (*15*) achieved an even smaller $R_{ON \cdot sp}$ = 1.25 $m\Omega \cdot cm^2$ with a device that had V_{BR} = 580 V. These values are almost an order of magnitude less than those of comparable SiC MOSFETs. The results are made even more impressive by the fact that they were fabricated on device structures grown on Si, which has an even larger mismatch than sapphire. The attraction of the Si substrate, of course, is that it is much less expensive and very large diameter wafers are available. However, these devices still have reliability issues. It is also difficult to make a normally-off device, but the record setting IMEC HEMT is a normally-off device. The devices are also lateral devices with front side contacts, which should limit the ability to achieve large breakdown voltages and high current carrying capacities. However,

Panasonic has achieved V_{BR} = 10.4 kV, and scientists at Furukawa Electric have achieved i = 120 A with V_{BR} > 1.8 kV, while researchers at Sankin have obtained i = 170 A with V_{BR} = 750 V.

In our initial studies we have learned how to fabricate HEMTs from device structures grown on sapphire and Si because they are the cheaper substrates, and so we can compare our results with those in the literature. We have been able to demonstrate we have 2DEGs in both structures, and we have fabricated and tested devices. For the devices fabricated on sapphire we achieved a 2DEG carrier concentration of 2 x 10^{13} cm^{-2}, which is a good result. As expected, the 2DEG concentration in the devices on Si were lower, about an order of magnitude, because the device structure on Si contains more defects due, in part, to the lattice mismatch. The devices on the Si substrates also had a larger gate leakage and a smaller transconductance. Note in figure 12, that people have to go to extraordinary measures to reduce the effects of the lattice mismatch by growing a transition AlGaN buffer layer.

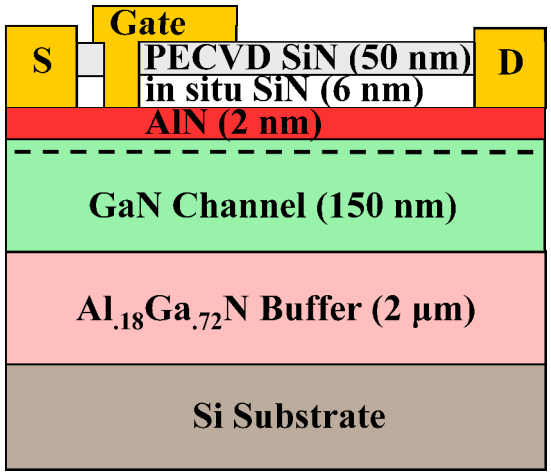


Figure 12. Schematic of a lateral high power electronic HEMT.

Now that we have established that we can fabricate HEMTs, we will begin to fabricate them on HVPE substrates, and, if that proves to be beneficial, we will then try to make them using the high quality crystals from Poland. Since the GaN substrates are conducting substrates, we will also attempt to make vertical devices.

4. Future Work

Looking to the future, we expect to expand our GaN work to include AlGaN because AlN has significantly better parameters than either GaN or SiC. Because E_G = 6.2 eV for AlN is almost twice that of the other two, its ξ_C = 11.7 MV/cm (*16*) is much larger. This is offset to some extent by its smaller electron mobility, thought to be 426 $cm^2/V{\cdot}s$ (*17*), but it still has a much

higher FOM, as shown in figure 13, because the FOM α V_{BR}^2. There is some concern that the Si donor level is too deep, but it has recently been determined to have a depth of only 65–75 meV (*18*) , which is significantly smaller than the depth of the Mg acceptor in GaN, which is ~120 meV. Also, high quality crystals are already being grown because it is actually easier to grow them than GaN crystals, due to the fact that the N vapor pressure is much less than it is for GaN – the Al-N bond is much stronger. Most likely there will be compromises and AlGaN will be used. AlGaN is not lattice matched to either GaN or AlN crystals, so it is essential that we learn how to grow AlGaN on GaN like they do SiGe on Si, be it by graded junction or a stepped superlattice (*6*).

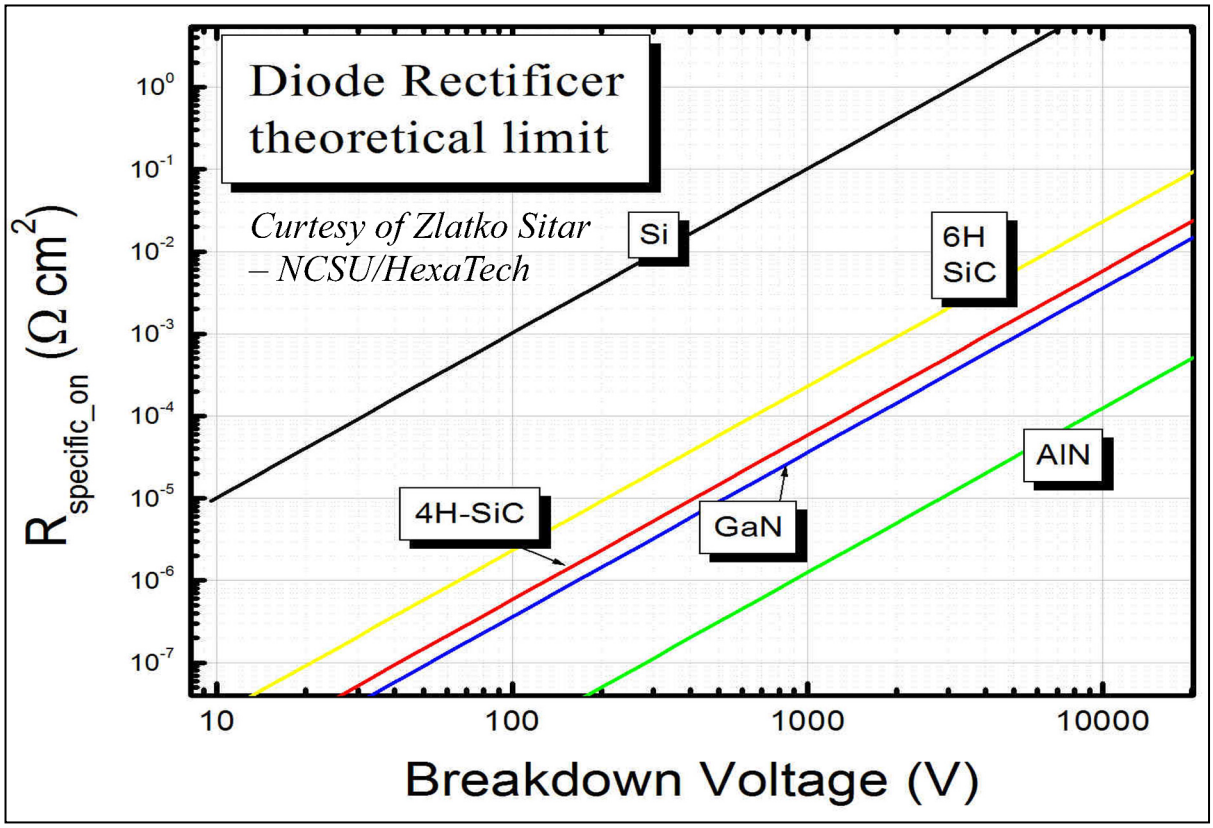


Figure 13. Plot of the ideal breakdown voltage as a function of the specific on resistance for AlN, as well as for Si, SiC, and GaN.

5. Conclusions

Great strides have been made in the fabrication and understanding of the operation of SDs. We achieved our goal of making diodes with V_{BR} > 600 V, which is the first plateau for HPE diodes; e.g., it is the buss voltage for DC → AC inverters in electrical vehicles. The largest value we obtained was V_{BR} = 704 V. We believe we are within reach of the record-setting work done by

researchers in Japan working over a number of years (*1*), and we hope to be able to meet or exceed their values of V_{BR} = 1100 V and FOM = 1.7 GW/cm^2, which is much better than the best achieved for SiC, and it even exceeds the best theoretical value.

Two key issues have been identified for us to be able to match or exceed these results. They are the C-background doping in MOCVD grown films and a high substrate resistance. It has been demonstrated that background C in MOCVD films acts as an acceptor hat compensates the Si n-type dopant, and the concentration is well in excess of 10^{16} cm^{-3}, which is the net donor concentration that must be reached to obtain V_{BR} ~ 1000 V. We have found through literature searches and experimentation that we should be able to reduce the C concentration below 10^{16} cm^{-3} by growing the GaN films at a higher pressure and growing them with fewer dislocations by growing them on GaN substrates. HVPE substrates and films grown on them have dislocation densities of ~10^6 /cm^2 compared to ~10^9/cm^2 dislocations in films currently being used. Single crystal substrates that we are in the process of purchasing from a company in Poland have only ~10^3/cm^2. Our smaller FOMs were due to a larger substrate resistance. We will be working with Kyma Technologies on growing more heavily doped HVPE substrates with funds from their Phase II Small Business Innovation Research (SBIR) contract. The crystals we have on order from Poland are conductive.

In supporting work we were unable to use the annealing process we are patenting to activate implanted p-type dopants, which is required to fabricate traditional JBS diodes with lower leakage currents than SDs. We showed experimentally that the ion implant process creates stacking faults, and the Mg dopants appear to stabilize them. We also theoretically showed that the stacking faults create deep donors that compensate the acceptors. However, we were able to improve the contact resistance for n-type contacts, achieving a record low value of 2.2 x $10^{-8}\Omega\cdot$cm^2. While this will not benefit SD work because the contact region is heavily doped, it could significantly improve operation of HPE HEMTs that we plan to make in the future. Currently, contacts are being made to low doped material. Using ion implantation, one can locally dope the contact region.

In parallel with demonstrating competitive SDs, we plan to fabricate and test HPE HEMTs that the Japanese have already showed have lower $R_{ON\cdot sp}$ than comparable SiC MOSFETs. We have begun the process and have demonstrated we can fabricate reasonably good HEMTs using sapphire and Si substrates. We anticipate that we will be able to greatly improve them using HVPE and solution grown GaN substrates. Looking out further, we plan to investigate AlGaN for higher power applications. The much larger ξ_C, a reasonable electron mobility and donor depth, and the availability of high quality AlN crystals suggest this should be a good investment.

Exploiting the multi-scale modeling program, we also hope to learn how to grow AlGaN on GaN in such a way that the mismatch dislocations are confined to the region near the substrate/film interface away from the top surface where the critical parameters are the most sensitive to the negative effects of crystalline defects.

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List of Symbols, Abbreviations, and Acronyms

2DEG	two-dimensional electron gas
AFM	atomic force microscopy
Al	aluminum
Al_2O_3	sapphire
AlGaN	aluminum gallium nitride
AlN	aluminum nitride
ARL	U.S. Army Research Laboratory
As	arsenic
AsH_3	arsine
C	capacitance
C	carbon
$[(CH_3)_3Ga]$	organometallic, trimethyl gallium
CL	cathodoluminescence
DFT	density functional theory
DRI	Director's Research Initiative
DSI	Director's Strategic Initiative
ECCI	electron channeling contrast imaging
E_F	Fermi energy
E_G	energy gap
FOM	figure of merit
GaAs	gallium arsenide
GaCl	gallium chloride
GaN	gallium nitride
Ge	germanium

H	hydrogen
HEMT	high electron mobility transistor
HPE	high power electronic
HVPE	hydride vapor phase epitaxy
i	current
I_o	ideal reverse saturation current
JBS	junction barrier Schottky
k	Boltzmann's constant
KOH	potassium hydroxide
LAGB	low angle grain boundary
MBE	molecular beam epitaxy
Mg	magnesium
MOCVD	metal-organic chemical vapor deposition
MOSFET	metal-oxide-semiconductor field effect transistor
N_2	nitrogen
n	semiconductor ideality factor
n_{dmx}	theoretical maximum donor doping concentration for a given V_B
NH_3	ammonia
O	oxygen
q	charge on an electron
RF	radio frequency
RFOM	relative figure of merit
$R_{ON \cdot sp}$	specific on-resistance
SBIR	Small Business Innovation Research
SD	Schottky diode
SEM	scanning electron microscopy
Si	silicon

SiC	silicon carbide
SiGe	silicon-germanium
SiH_4	silane
SIMS	secondary ion mass spectroscopy
SiO_2	silicon dioxide
SUNY	State University of New York
T	temperature
T_A	annealing temperature
Ti	titanium
UID	unintentionally doped
UV	ultraviolet
V	voltage
V_B	breakdown voltage
W_B	depletion layer width at breakdown
ξ_C	critical electric field
ε	electric permittivity
$ø_b$	Schottky diode barrier height
ρ_c	specific contact resistance
μ	electron mobility

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